**Amendment to the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application. The following listing provides the amended claims with the amendments marked with deleted material crossed out and new material underlined to show the changes made.

Claims 1-27 (Canceled).

28. (Currently Amended) For a placer that places circuit modules in integrated-circuit ("IC") layouts, the placer using a set of partitioning lines, that define a plurality of slots, to partition an IC layout region into a plurality of sub-regions corresponding to said slots, a method of pre-computing costs of placing circuit modules in an IC-layout region, the method comprising:

a) selecting a first group of said slots;

b) computing a first attribute of a set of one or more interconnect lines necessary for connecting the first group of said slots, wherein computing the first attribute comprises calculating the length of said set of interconnect lines;

c) computing a second attribute of the set of interconnect lines, wherein said second attribute comprises the number of bends in said set of interconnect lines; and

d) storing the computed attributes in a storage structure for later use by said placer during a placement operation.

29. (Canceled)

30. (Cancel)

31. (Currently Amended) The method of claim ~~30~~28 wherein the bends are diagonal

bends.

32. (Original) The method of claim 28, wherein a plurality of line paths exist between said slots, wherein computing the first attribute comprises identifying the line paths used by said set of interconnect lines.

33. (Original) The method of claim 28, wherein a plurality of edges exist between said slots, wherein computing the first attribute comprises identifying the edges intersected by said set of interconnect lines.

34. (Currently Amended) The method of claim 28 further comprising:

~~a~~e) computing a third attribute of the set of interconnect lines; and

~~b~~f) storing the computed third attributes in the storage structure.

35. (Currently Amended) The method of claim 28 further comprising:

~~a~~e) selecting a second group of said slots different from said first group;

~~b~~f) computing first and second attributes of a set of one or more interconnect lines connecting the second group of said slots;

~~e~~g) storing the computed attributes in the storage structure.

36. (Currently Amended) For an electronic design automation ("EDA") application that performs placement operations, a method of pre-computing costs of placing circuit elements within an integrated-circuit ("IC") layout, the method comprising:

a) defining a partitioning grid having a plurality of slots, said partitioning



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grid for partitioning a region of an IC layout during a placement operation;

b) for each combination of said slots, defining at least one connection graph that models the topology of interconnect lines necessary for connecting the combination of said slots;

c) computing multiple attributes for each of said connection graphs, wherein one of said attributes comprises the number of bends in each connection graph of a plurality of said connection graphs;

d) storing the computed attributes in a storage structure for later use by said EDA application during said placement operation.

37. (Original) The method of claim 36, wherein the connection graphs are Steiner trees.

38. (Original) The method of claim 36, wherein the connection graphs are minimum spanning trees.

39. (Original) The method of claim 36, wherein computing multiple attributes of each connection graph comprises calculating the length of each graph.

40. (Cancel)

41. (Currently Amended) The method of claim ~~40~~36, wherein the bends are diagonal bends.

42. (Original) The method of claim 36, wherein the partitioning grid having a

plurality of edges between said slots, wherein computing multiple attributes of each connection graph comprises identifying the edges intersected by each graph.

43. (Original) The method of claim 42, wherein said partitioning grid having a particular structure, wherein said edges are defined based on a wiring model for the IC layout and on the structure of the partitioning grid.

44. (Original) The method of claim 36, wherein the partitioning grid having a plurality of interconnect-line paths between said slots, wherein computing multiple attributes of each connection graph comprises identifying the paths used by each graph.

45. (Original) The method of claim 44, wherein said partitioning grid having a particular structure, wherein said interconnect-line paths are defined based on a wiring model for the IC layout and on the structure of the partitioning grid.

46. (Original) The method of claim 36, wherein the partitioning grid having a plurality of interconnect-line paths between said slots, wherein computing multiple attributes of each connection graph comprises calculating the length of each graph and identifying the paths used by each graph.

47. (Original) The method of claim 36, wherein the partitioning grid having a plurality of edges between said slots, wherein computing multiple attributes of each connection graph comprises calculating the length of each graph and identifying the edges intersected by each graph.

48. (Original) The method of claim 36, wherein the partitioning grid is formed by

a set of partitioning lines.

49. (Original) The method of claim 48, wherein the partitioning lines are horizontal and vertical lines.

50. (Currently Amended) For an electronic design automation ("EDA") application that performs placement operations, a method of pre-computing costs of placing circuit elements within an integrated-circuit ("IC") layout, the method comprising:

a) defining a partitioning grid having a plurality of slots, said partitioning grid for partitioning, during a placement operation, a region of an IC layout into a plurality of sub-regions corresponding to said slots;

b) for each combination of said slots, identifying at least one connection graph that models the topology of interconnect lines necessary for connecting the combination of said slots;

c) computing the length and number of bends in each of said connection graphs;

d) ~~for each particular combination of said slots,~~ storing the length of a connection graph identified for ~~that particular~~ each combination of said slots, wherein when more than one connection ~~graphs are~~ graph is defined for ~~that~~ a particular combination of said slots, the method storing the length of ~~shortest~~ a short connection graph that has less than a first predetermined number of bends.

51. (Currently Amended) The method of claim 50 further comprising:

for each ~~particular~~ combination of said slots that has more than one identified connection ~~graphs~~graph, storing the length of ~~shortest~~ a short connection graph that has less than a second predetermined number of bends, when none of the connection graphs for the particular combination of said slots have less than the first predetermined number of bends.

52. (Currently Amended) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC region into several sub-regions;

b) selecting a net;

c) identifying the set of sub-regions containing the circuit elements of the selected net~~;~~;

d) retrieving from a storage structure multiple pre-computed attributes of a set of one or more interconnect lines necessary for connecting the identified set of sub-regions;

e) computing a placement cost of said net within said region by using the retrieved attributes;

f) changing the position of a circuit element of the net from one sub-region to another;

g) identifying a new set of sub-regions that contain the circuit elements of the net;

h) retrieving multiple pre-computed attributes of a different set of interconnect lines necessary for connecting the identified new set of sub-regions; and

i) computing a new placement cost of said net within said region by using the attributes retrieved for the different set of interconnect lines, wherein said retrieved attributes include the number of bends in said different set of interconnect lines.

53. (Canceled)

54. (Currently Amended) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC-layout region into several sub-regions;

b) for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net;

c) for each particular net, retrieving multiple pre-computed attributes of a connection graph that models the topology of interconnect lines needed to connect the identified set of sub-regions of the particular net, wherein the connection graph is either a Steiner tree or a minimum spanning tree;

d) computing a placement cost for the IC layout within said region by using the retrieved attributes, wherein said retrieved attributes include the number of bends in a plurality of said connection graphs.

55. (Canceled)

56. (Canceled)